Multilevel transition in empty substrate integrated waveguide

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Empty Substrate Integrated Waveguide (ESIW) is an improvement of the well known Substrate Integrated Waveguide (SIW). While maintaining the low cost, easy manufacturing, small size, and integration with other circuits in the same substrate, ESIW decreases the related losses by removing the dielectric substrate, thus rendering it more interesting for practical applications. A wide band transition has been already developed to connect ESIW to microstrip lines. Filters, couplers and antennas have also been developed in ESIW. For multilevel configurations, where different ESIW devices are implemented in different stacked substrates, a transition is needed that connects ESIW lines in different substrate levels. In this work a low reflection wideband transition is presented for connecting two stacked ESIW lines.

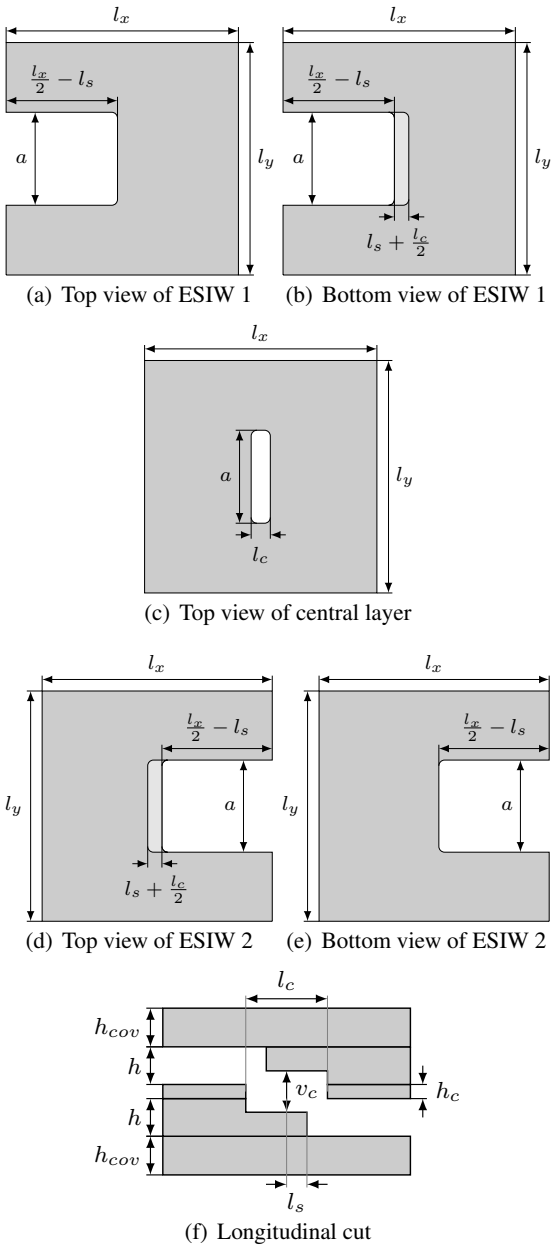
Introduction: The Empty Substrate Integrated Waveguide (ESIW) [1] was the first waveguide integrated in a substrate that improved significantly the performance of the well known substrate integrated waveguides (SIW) by removing the dielectric, and thus decreasing the related insertion losses. There is a growing interest in ESIW, since other implementations have appeared recently (the hollow substrate integrated waveguide (HSIW) [2], the air filled substrate integrated waveguide [3], the dielectricless substrate integrated waveguide presented in [4], and the empty substrate integrated coaxial line (ESICL) [5]).

The ESIW has already been successfully tested with the design and manufacturing of coupled cavity filters with very high quality factors [1], a horn antenna [6], and a hybrid directional coupler [7]. In all these devices, a wideband transition has been used to connect the ESIW to accessing microstrip lines. However, for multilevel configurations, where different ESIW devices are implemented in different stacked substrates, a transition in needed that connects ESIW lines in different substrate levels.

In this work a wideband and low reflection transition that connects two stacked ESIW lines (placed in different layers) is presented.

Stacked ESIW: An ESIW line consists of an emptied and metallized substrate closed with a top and a bottom metallic layers that act as the top and bottom walls of the waveguide (see [1]). The transition between two stacked ESIW is composed of a top and a bottom cover of height h_{cov}, two emptied substrates (one for each ESIW) of height h, and a central layer with a coupling slot that couples both ESIW lines of height h_c, as shown in figure 1(f). It can be observed that the central layer (see figure 1(c) and figure 1(f)) has a coupling slot of width a and length l_c, where a is the width of the ESIW lines (see figures 1(a) and 1(d)). All the layers of the transition are of length l_x and width l_y. In order to improve the matching, the substrates of height h, where the ESIW lines of width a are mechanized, are lowered near the slot. They are lowered in height by $(v_c - h_c)/2$, a distance $l_s + l_c/2$ (see figures 1(f), 1(b) and 1(d)), so that the waves traveling through the first ESIW line find an stair-like path that leads to the other ESIW line when they reach the coupling slot (see figure1(f)). When the geometrical dimensions are optimized, this stair-like path greatly minimizes the reflections and the return losses.

Figure 2 shows the 3D view of the transition modeled with the full wave simulator Computer Science Technology (CST), and the assembling of the five layers can be observed. Figure 2(a) shows the transition with only the bottom cover and the bottom ESIW line. The transition from ESIW to microstrip at the end of the ESIW line can be observed [1]. It can also be observed how the ESIW line ends in a short circuit, but the height of this short circuit is lowered at the beginning (a distance $l_s + l_c/2$ as shown in figure 1(d)), in order to improve the matching. Figure 2(b) shows the transition when the central layer is stacked. The coupling slot of dimensions $a \times l_c$ can be observed. The mechanization with a drill machine produces rounded corners. The radius of these rounded corners (0.5 mm) is the radius of the drill used for mechanizing. Figure 2(c) shows the transition when the top ESIW line has been added. In this top view can not be observed, but this layer has also been lowered in the bottom view (as shown in figure 1(b)). Finally, figure 2(d) shows the whole transition when the top cover has also been assembled.



(a) Top view of ESIW 1 (b) Bottom view of ESIW 1

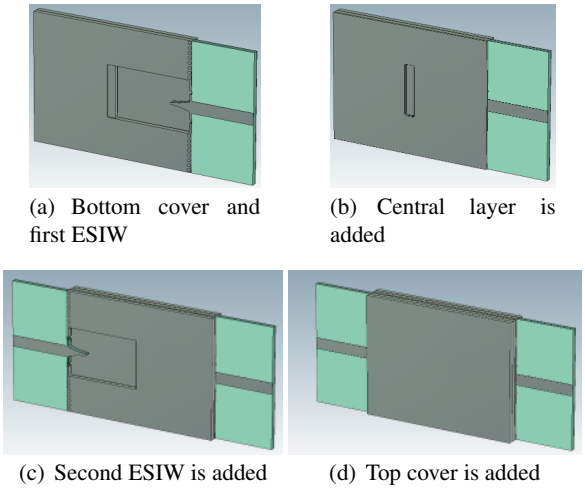
(c) Top view of central layer

(d) Top view of ESIW 2 (e) Bottom view of ESIW 2

(f) Longitudinal cut

Fig. 1 *Layout of the different layers of the multilevel transition. Light gray represents the copper metallization on both layers; black represents the metallization of the lateral walls; and white is air.*

Design: A transition has been designed for an ESIW line of the same width as the WR-62 ($a = 15,799$ mm). The design goal is to minimize the return loss in all the usable frequency band of the WR-62 (from 12 to 18 GHz). Rogers 4003C substrates of $_r = 3,55$ have been used for the two ESIW layers and also for the central layer. The substrate height for the ESIW layers is $1,524$ mm, and $0,508$ mm for the central layer. FR4 substrates of height $1,5$ mm have been used for the top and bottom covers. All the substrates come with a copper foil of $35\,\mu$m of thickness, but after being drilled an additional layer of $25\,\mu$m of electrodeposited copper is added. Consequently, the heights of all the layers are $h = 1,524 + 2 \cdot 0,035 + 2 \cdot 0,025 = 1,644$ mm, $h_c = 0,508 + 2 \cdot 0,035 + 2 \cdot 0,025 = 0,628$ mm, and $h_{cov} = 1,5 + 2 \cdot 0,035 + 2 \cdot 0,025 = 1,62$ mm, as shown in table 1. In this table the chosen values for the width and length of all the layers (l_x and l_y) is also shown. The rest of the parameters of table 1 (l_c, l_s and v_c) are the design parameters. Using the CST simulator, these parameters have been optimized with the goal of minimizing the return losses in all the usable frequency band. The resulting optimized values are the ones presented in table 1.



(a) Bottom cover and first ESIW

(b) Central layer is added

(c) Second ESIW is added

(d) Top cover is added

Fig. 2 *Schematic 3D views of the stacked ESIW transition, with the assembling procedure of the 5 layers. (a) Bottom cover and first ESIW line. (b) Central layer is added. (c) Second ESIW is added. (d) Top cover is added and the assembling is completed*

Results: Figure 3 shows the manufactured prototype before assembling. The five layers can be observed. All the layers have been drilled with holes for alignment screws. Tin soldering paste is placed between adjacent layers and then it is dried in a reflow oven. Once the soldering paste is dried, the alignment screws are removed.

Once assembled, the manufactured prototype of figure3 has been measured with a network analyzer. Measurements and simulated results are compared in figure 4. There is a good agreement between simulation and measurements. Measured return losses are above 18 dB in all the usable frequency band. Insertion losses are below 1 dB.

l_x	l_y	a	l_c	l_s
40	39.05	15.7988	3.3237	0.8209
v_c	h	h_{cov}	h_c	
1.6735	1.644	1.62	0.628	

Table 1: Dimensions of the multilevel transition (all dimensions in mm)

Fig. 3. Vertically stacked ESIW before assembling.

Conclusion: A novel transition for multilevel ESIW configurations has been presented. The transition is simple to manufacture and design. A prototype has been manufactured for an ESIW of the same width as the WR-62. Measured return losses are above 18 dB and insertion loss below 1 dB in all the usable frequency band of the ESIW.

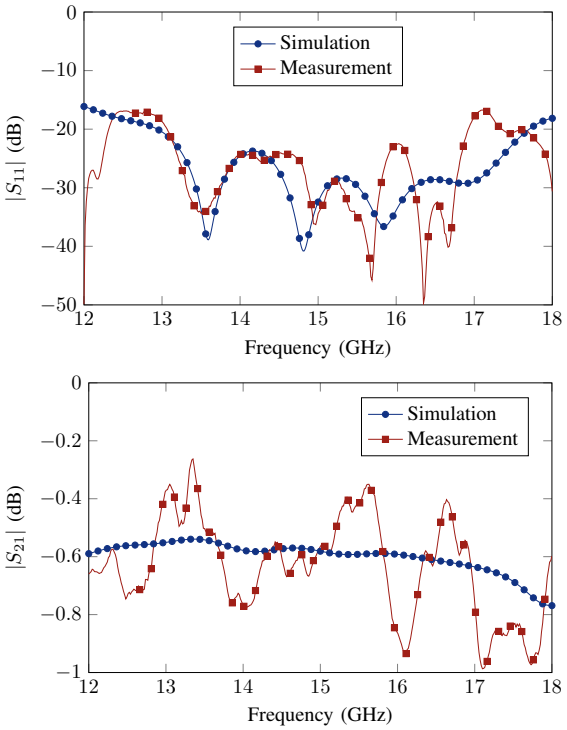


Fig. 4 *Comparison between simulation and measurements for the manufactured stacked ESIW transition*

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